Claims

[c1] 1.A method of isolating a defect in a scan chain comprising:
modifying a first test mode of one or more of a plurality of latches included in the scan chain;
operating the one or more latches whose first test modes are modified in the modified first test mode; and
operating one or more of the plurality of latches included in the scan chain in a second test mode.

[c2] 2.The method of claim 1 wherein modifying the first test mode of one or more of the plurality of latches included in the scan chain includes modifying the first test mode of one or more of the plurality of latches included in the scan chain such that adjacent portions of a non-defective section of the scan chain store complementary signals when the one or more latches whose first test modes are modified are operated in the modified first test mode, wherein a portion includes at least one of one or more latches, one or more macros, and one or more partitions of a macro.

[c3] 3.The method of claim 1 wherein operating the one or more latches whose first test modes are modified in the

modified first test mode includes operating the one or more latches whose first test modes are modified in a modified flush test mode.

[c4] 4.The method of claim 1 wherein operating one or more latches whose first test modes are modified in the modified first test mode includes initializing the value stored in the one or more latches whose first test modes are modified such that adjacent portions in a non-defective section of the scan chain store complementary signals, wherein a portion includes at least one of one or more latches, one or more macros, and one or more partitions of a macro.

[c5] 5.The method of claim 1 wherein operating one or more of the plurality of latches included in the scan chain in the second test mode includes operating one or more of the plurality of latches included in the scan chain in a scan mode.

[c6] 6.The method of claim 1 wherein operating one or more of the plurality of latches included in the scan chain in the second test mode includes unloading data from the scan chain.

[c7] 7.A method of isolating a defect in a scan chain comprising:

modifying a first test mode of one or more of a plurality of latches included in the scan chain;
while inputting a first value to the scan chain, operating the one or more latches whose first test modes are modified in the modified first test mode to store a first set of data in the scan chain;
operating one or more of the plurality of latches included in the scan chain in a second test mode to output the first set of data;
while inputting a second value to the scan chain, operating the one or more latches whose first test modes are modified in the modified first test mode to store a second set of data in the scan chain;
operating one or more of the plurality of latches included in the scan chain in the second test mode to output the second set of data; and
employing the first set of data and the second set of data to isolate a defect in the scan chain.

[c8] 8.A method of testing and diagnosing a scan chain comprising:
altering the function of the scan chain flush test mode; and
employing the flush test mode to test and diagnose the scan chain.

[c9] 9.The method of claim 8 further comprising employing a scan mode to test and diagnose the scan chain.

[c10] 10.The method of claim 8 wherein altering the function of the scan chain flush test mode includes altering the function of the scan chain flush test mode such that an alternating set of complementing states are propagated through the scan chain.

[c11] 11.The method of claim 8 wherein altering the function of the scan chain flush test mode includes altering the scan chain path input to one or more latches included in the scan chain such that the one or more latches write the scan input when the flush test mode is employed.

[c12] 12.An integrated circuit (IC) for isolating a defect in a scan chain comprising:
a plurality of latches included in the scan chain; and
one or more logic devices coupled to the plurality of latches included in the scan chain;
wherein the IC is adapted to:
modify a first test mode of one or more of the plurality of latches included in the scan chain;
operate the one or more latches whose first test modes are modified in the modified first test mode; and
operate one or more of the plurality of latches included in the scan chain in a second test mode.

[c13] 13.The IC of claim 12 wherein the IC is further adapted to modify the first test mode of one or more of the plurality of latches included in the scan chain such that adjacent portions of a non-defective section of the scan chain store complementary signals when the one or more latches whose first test modes are modified are operated in the modified first test mode, wherein a portion includes at least one of one or more latches, one or more macros, and one or more partitions of a macro.

[c14] 14.The IC of claim 12 wherein the IC is further adapted to operate the one or more latches whose first test modes are modified in a modified flush test mode.

[c15] 15. The IC of claim 12 wherein the IC is further adapted to initialize the value stored in the one or more latches whose first test modes are modified such that adjacent portions in a non-defective section of the scan chain store complementary signals, wherein a portion includes at least one of one or more latches, one or more macros, and one or more partitions of a macro.

[c16] 16.The IC of claim 12 wherein the IC is further adapted to operate one or more latches of the plurality of latches included in the scan chain in a scan mode.

[c17] 17.The IC of claim 12 wherein the IC is further adapted

to unload data from the scan chain.

[c18] 18.The IC of claim 12 wherein at least one of the one or more logic devices is coupled to a scan input of one or more of the plurality of latches included in the scan chain.

[c19] 19.The IC of claim 18 wherein at least one of the plurality of latches includes an L1 latch coupled to an L2 latch; and
wherein at least one of the one or more logic devices is coupled to an output of one or more of the L1 latches.

[c20] 20.An integrated circuit (IC) for isolating a defect in a scan chain comprising:
a plurality of latches included in the scan chain; and
one or more logic devices coupled to the plurality of latches included in the scan chain;
wherein the IC is adapted to:
modify a first test mode of one or more of a plurality of latches included in the scan chain;
while inputting a first value to the scan chain, operate the one or more latches whose first test modes are modified in the modified first test mode to store a first set of data in the scan chain;
operate one or more of the plurality of latches included in the scan chain in a second test mode to output the

first set of data;
while inputting a second value to the scan chain, operate the one or more latches whose first test modes are modified in the modified first test mode chain to store a second set of data in the scan chain;
operate one or more of the plurality of latches included in the scan chain in the second test mode to output the second set of data; and
employ the first set of data and the second set of data to isolate a defect in the scan chain.

[c21] 21.An integrated circuit (IC) for testing and diagnosing a scan chain comprising:
a plurality of latches catenated into the scan chain; and
one or more logic devices coupled to the scan chain;
wherein the IC is adapted to:
alter the function of the scan chain flush test mode; and
employ the flush test mode to test and diagnose the scan chain.

[c22] 22.The IC of claim 21 wherein the IC is further adapted to employ a scan mode to test and diagnose the scan chain.

[c23] 23.The IC of claim 21 wherein the IC is further adapted to alter the function of the scan chain flush test mode such that an alternating set of complementing states are

propagated through the scan chain.

[c24] 24.The IC of claim 21 wherein the IC is further adapted to alter the function of the scan chain flush test mode using the one or more logic devices such that an alternating set of complementing states are propagated through the scan chain.

[c25] 25.The IC of claim 21 wherein the IC is further adapted to alter the scan chain path input to one or more latches such that the one or more latches write the scan input when the flush test mode is employed.

[c26] 26.The IC of claim 21 wherein the IC is further adapted to alter the scan chain path input to one or more latches using one or more logic devices such that the one or more latches write the scan input when the flush test mode is employed.

[c27] 27.The method of claim 1 wherein the scan chain is a level sensitive scan design (LSSD) scan chain.

[c28] 28.The method of claim 7 wherein the scan chain is a level sensitive scan design (LSSD) scan chain.

[c29] 29.The method of claim 8 wherein the scan chain is a level sensitive scan design (LSSD) scan chain.

[c30] 30.The IC of claim 12 wherein the scan chain is a level

sensitive scan design (LSSD) scan chain.

[c31] 31.The IC of claim 20 wherein the scan chain is a level sensitive scan design (LSSD) scan chain.

[c32] 32.The IC of claim 21 wherein the scan chain is a level sensitive scan design (LSSD) scan chain.